profpga
Speed meets Flexibility

uno XCVU19P Prototyping System

Product Summary

The proFPGA uno XCVU19P system is a complete and modular multi-FPGA solution, which meets highest requirements in the area of FPGA based Prototyping. It addresses customers who need a scalable and flexible high speed ASIC Prototyping solution for early software development and real time system verification. The innovative system concept offers highest flexibility and reusability reconfigurability for several projects, which guarantees the best return on investment.

Highest Flexibility

The system architecture is based on a modular and scalable single-chip concept. The FPGAs are assembled on dedicated FPGA modules, which will be plugged on the proFPGA uno, duo or quad motherboard. This offers the highest flexibility to use for example different FPGA types in one system or to scale a system in increments of one FPGA. The user has access to almost all I/Os of the FPGA, which gives him maximum freedom regarding the FPGA interconnection structure. This way the prototyping system can be adapted in the best way to any user design. Furthermore the system offers a total of 56 extension sites on the top and bottom site for standard or user specific extension boards like DDR4 memory, PCIe gen1/2/3, Gigabit Ethernet, USB 3.0 or other high speed interface and interconnect boards.

Maximum Performance

The well designed boards of the proFPGA system are optimized and trimmed to guarantee best signal integrity and to achieve highest performance. The high speed boards together with specific high speed connectors allow a maximum point-to-point speed of up to 1.0 Gbps single ended over the standard FPGA I/Os and up to 28 Gbps differential over the high speed serial transceivers of the FPGA. This performance combined with the high interconnection flexibility allows the designer to run his design at the highest possible speed in the proFPGA system.

Biggest Capacity

Equipped with one Xilinx Virtex® UltraScale+™ VU19P FPGA module, the proFPGA uno system can handle up to 48 M ASIC gates on the board.

Very User Friendly

The proFPGA prototyping system provides an extensive set of features and tools, like remote system configuration, integrated self and performance test, automatic board detection, automatic I/O voltage programming, system scan and safety mechanism, which simplifies the usage of the FPGA based system tremendously.

VIRTEX UltraSCALE+

SST Smart Stacking Technology · FMT FPGA Mixing Technology · DMBI Device Message Box Interface · ACM Advanced Clock Management

Key Features

- 48 M ASIC gates capacity on one board
- 1932 user I/O
- 48 dedicated high speed serial transceivers
- 14 individually adjustable voltage regions
- Up to 1.0 Gbps single ended point-to-point speed
- proFPGA FPGA Mixing Technology (FMT)
- Smart Stacking Technology (SST)
- High performance host interface (DMBI)
- Advanced Clock Management (ACM)

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Innovative Technologies

SST
Smart Stacking Technology

Smart Stacking Technology

- Board detection when boards are plugged
- Automatic and right I/O voltage setting and programming with conflict detection
- Integrated interconnection self and performance test
- Smart I/O resource management. No I/O resources get lost or blocked by connectors

FMT
FPGA Mixing Technology

FPGA Mixing Technology

- Easy plugging and unplugging of FPGA modules on motherboards
- Various FPGAs from different vendors can be mixed
- Automatic scan and detection of FPGA modules, when plugged
- Different FPGA configurations are controlled by proFPGA Builder Software

DMBI
Device Message Box Interface

Device Message Box Interface

- High speed, low latency data exchange system
- Enables various use modes and functionalities like remote system configuration and monitoring, de bug, application level program-ming and co-simulation
- Up to 3.5 Gbps data transfer rate
- Runs over USB, Ethernet or PCIe

ACM
Advanced Clock Management

Advanced Clock Management

- Run-time configurable local clocks
- Each clock with sync signals
- 6 fixed clocks

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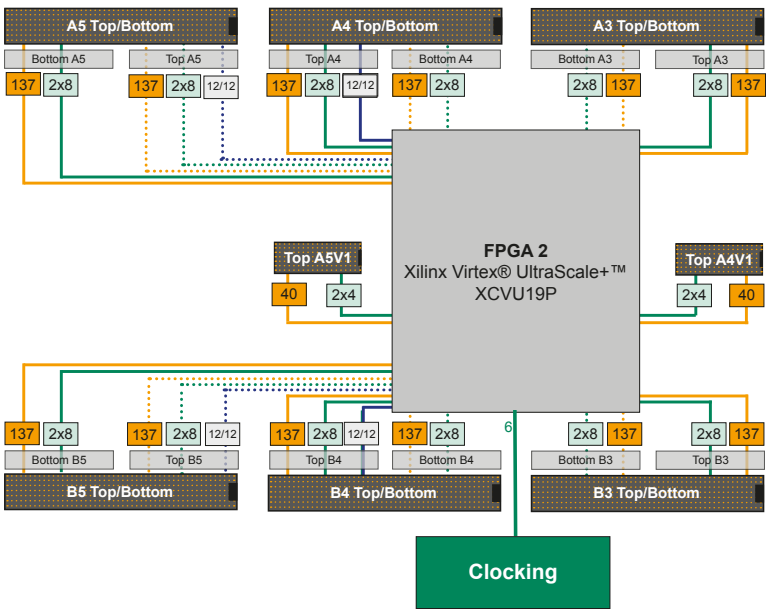
profpga uno XCVU19P Specification	
FPGAs	- 1 x Xilinx Virtex XCVU19P FPGA Modules
Capacity	- Up to 48 M ASIC gates
FPGA-internal memory	- Up to 75 Mbits on the board
Signaling rate	- Up to 1.0 Gbps (standard I/O)/ up to 28 Gbps (MGT)
Extension sites	- Up to 14 Extension sites with high speed connectors
I/O resources	- Overall 1932 free I/Os per FPGA Module - 6 x 153 I/Os and 2 x 48 I/Os to top side connectors - 6 x 153 I/Os bottom side connectors
High speed I/O transceivers	- Overall 48 high speed transceivers (28 Gbps) on top and bottom side
FPGAs interconnections	- Flexible via high-speed interconnection boards or cables
Voltage regions	- 14 individually adjustable I/O voltage regions - Stepless from 1.2V up 1.8V - Automated detection of daughter cards and setting of right voltages
Clocking	- 6 fixed global clock and sync inputs per connector - use of up to 6 clock-capable I/Os per connector
Configuration	- With host software via Ethernet, USB, PCIe or Xilinx JTAG interface
Data exchange	- On board DMBI (Device Message Box Interface) - Data exchange rate: - Ethernet (up to 100 Mbps), USB (480 Mbps), PCIe (up to 3.5 Gbps)
Power	External (optional) ATX Power Supply (12 V, 24 - 35 A output)
Dimensions	- 5.91" x 0.95" x 5.91" / 150 mm x 24 mm x 150 mm (width x height x depth) - 0.5 kg weight

profpga uno I/O and Clock Architecture



Signal Types
IO — IO/Clock — GTH (tx/rx)

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