uno VUS 440 Prototyping System

Product Summary

The proFPGA uno VUS 440 system is a complete and modular FPGA solution, which meets highest requirements in the area of FPGA based Prototyping. It addresses customers who need a scalable and flexible high speed ASIC Prototyping and IP verification solution for early software development and real time system verification. The innovative system concept offers highest flexibility and reusability, reconfigurability for several projects, which guarantees the best return on invest.

Highest Flexibility

The system architecture is based on a modular system concept. The FPGAs are assembled on dedicated FPGA modules, which will be plugged on the proFPGA uno, duo or quad motherboard. This offers the highest flexibility to use for example different FPGA types in one system. The user has nearly 100% access to all available I/Os of the FPGA, which gives him maximum freedom regarding the FPGA interconnection structure. This way the prototyping system can be adapted in the best way to any user design. Furthermore the system offers a total of 10 extension sites on the top and bottom site for standard proFPGA or user specific extension boards like DDR-4 memory, PCIe gen1/2/3, Gigabit Ethernet, USB 3.0 or other high performance interface.

Maximum Performance

The well designed boards of the proFPGA system are optimized and trimmed to guarantee best signal integrity and to achieve highest performance. The high speed boards together with specific high speed connectors allow a maximum point to point speed of up to 1.0 Gbps single ended over the standard FPGA I/O and up to 12.5 Gbps differential over the high speed serial transceivers of the FPGA. This performance combined with the high interconnection flexibility allows the designer to run his design at maximum speed in the proFPGA system.

Biggest Capacity

Equipped with one Xilinx Virtex UltraScale 440 FPGA module, the proFPGA uno system can handle up to 30 M ASIC gates on only one board.

Very User Friendly

The proFPGA prototyping system provides an extensive set of features and tools, like remote system configuration, integrated self and performance test, automatic board detection, automatic I/O voltage programming, system scan and safety mechanism, which simplifies the usage of the FPGA based system tremendously.

XILINX UltraSCALE

SST Smart Stacking Technology · FMT FPGA Mixing Technology · DMBI Device Message Box Interface · ACM Advanced Clock Management

Key Features

- 30 M ASIC gates capacity on one board
- 1327 signals for I/O and inter FPGA connection
- 48 dedicated high speed serial I/O transceivers
- 10 individually adjustable voltage regions
- Up to 1.0 Gbps single ended point to point speed
- Up to 12.5 Gbps speed differential over MGTs
- Smart Stacking Technology (SST)
- High performance host interface (DMBI)
- proFPGA Builder Software

uno VUS 440 Prototyping System

profpga
Speed meets Flexibility

Innovative Technologies

SST
Smart Stacking Technology

Smart Stacking Technology

- Board detection when boards are plugged
- Automatic and right I/O voltage setting and programming with conflict detection
- Integrated interconnection self- and performance test
- Smart I/O resource management. No I/O resources get lost or get blocked by connectors

FMT
FPGA Mixing Technology

FPGA Mixing Technology

- Easy plugging and unplugging of FPGA modules on motherboards
- Various FPGAs from different vendors can be mixed
- Automatic scanning and detection of FPGA modules, when plugged
- Different FPGA configurations are controlled by proFPGA Builder software

DMBI
Device Message Box Interface

Device Message Box Interface

- High speed, low latency data exchange system
- Enables various use modes and functionalities like remote system configuration and monitoring, de bugging, application level program-ming and co-simulation
- Up to 3.5 Gbps data transfer rate
- Runs over USB, Ethernet or PCIe

ACM
Advanced Clock Management

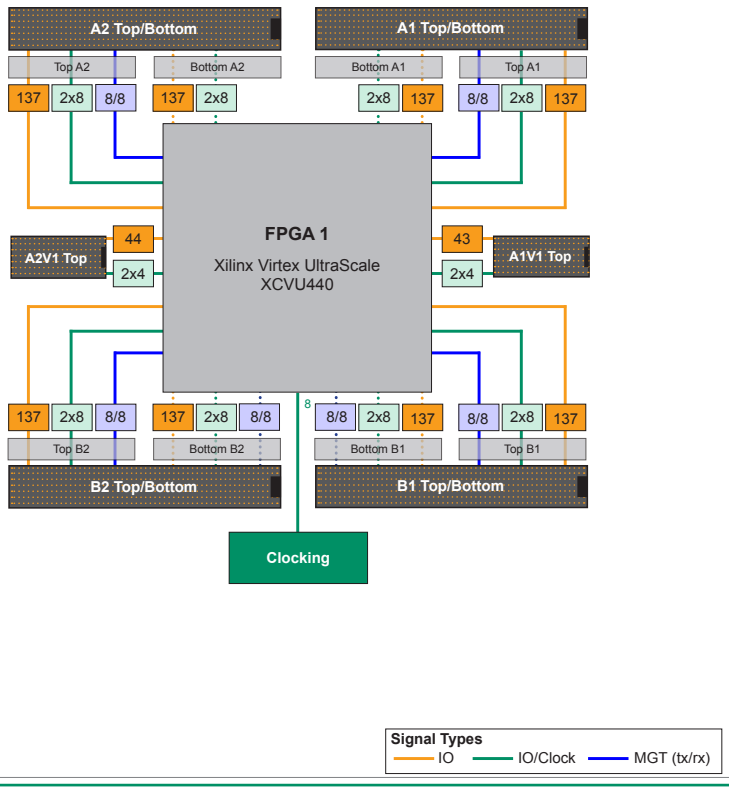
Advanced Clock Management

- 8 fixed clocks
- Run-time configurable local clocks
- Each clock with sync signals

profpga uno VUS 440 Specification

FPGAs	- 1 x Xilinx Virtex XCVU440 FPGA Module
Capacity	- 30 M ASIC gates on one board
FPGA-internal memory	- 88,600 kbits
Signaling rate	- Up to 1.0 Gbps single ended (standard I/O)/ up to 12.5 Gbps (MGT) differential
Extension sites	- 10 Extension sites with high speed connectors
I/O resources	- Overall 1327 signals for I/O and inter FPGA connection - 4x153 I/Os to top side connectors - 1x52 and 1 x 51 I/Os top side connectors - 4x153 I/Os to bottom side connectorsss
High speed I/O transceivers	- 48 dedicated MGTs running up to 12.5 Gbps - 4x8 MGTs to top side connectors - 2x8 MGTs to bottom side connectors
Available interface boards	- USB 3.0, PCIe Gen2/Gen3, MIPI, DVI, DDR3 memory, Gb Ethernet, etc.
Voltage regions	- 10 individually adjustable I/O voltage regions - Stepless from 1.0V up 1.8V on 9 extension sites - Stepless from 1.0V up 3.3V on one extension site - Automated detection of daughter card and adjustment of right voltage
Clocking	- 8 fixed clocks - 2 quartz as clock references - Run-time configurable local clocks - Fully synchronous derived clocks with sync signals
Configuration	- From host via Ethernet, USB or standalone over USB stick or Xilinx JTAG
Data exchange	- On board DMBI (Device Message Box Interface) - Data exchange rate: - Ethernet (up to 100 Mbps), USB (480 Mbps)
Power	External (optional) ATX Power Supply (12 V, 24 - 35 A output)
Dimensions	- 5.91" x 0.95" x 5.91" / 150 mm x 24 mm x 150 mm (width x height x depth) - 0.5 kg weight

profpga uno VUS 440 I/O and Clock Architecture



PRO DESIGN Electronic GmbH
Albert-Mayer-Str. 14 - 16
83052 Bruckmuehl, Germany

Phone:+49 (0) 8062-808-0
FAX: +49 (0) 8062-808-404
profpga@prodesign-europe.com

prodesign
the system solution provider